forming a second film in said first groove and thereafter removing said first film;

diffusing an impurity on a surface of said semiconductor substrate to form a grooved impurity diffusion region including a part of a bottom of said first groove by using said second film as a mask;

forming an insulator film on said grooved impurity diffusion region and thereafter removing said second film to form a second groove;

forming a gate insulator film in said second groove so that a top surface of said gate insulator film is arranged farther from said semiconductor substrate than a top surface of said grooved impurity diffusion region; and

forming a gate electrode on the top surface of said gate insulator film.

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15. (New) A method for producing a MIS transistor according to claim 14, wherein said second film is a semiconductor film, and further comprising:

forming a sacrificial film in said first groove before forming said second film in said first groove; and

removing said sacrificial film after removing said second film to form said second groove.

16. (New) A method for producing a MIS transistor according to claim 14, further comprising:

polishing a surface of said second film by using said first film as a stopper.

17. (New) A method for producing a MIS transistor according to claim 14, further comprising:

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forming a protective film in said second groove before forming said gate insulator film in said second groove.

18. (New) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the semiconductor substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

etching said semiconductor substrate to form a first groove by using said first film as a mask;

forming a second film in said first groove and thereafter removing said first film;

diffusing an impurity on a surface of said semiconductor substrate to form a grooved impurity diffusion region including a part of a bottom of said first groove by using said second film as a mask;

forming an insulator film on said grooved impurity diffusion region and thereafter removing said second film to form a second groove;

forming a gate insulator film in said second groove and on said insulator film;

polishing said gate insulator film by using said insulator film as a stopper so that a top surface of said gate insulator film is arranged farther from said semiconductor substrate than a top surface of said grooved impurity diffusion region; and

forming a gate electrode on the top surface of said gate insulator film.

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19. (New) A method for producing a MIS transistor according to claim 18, wherein said second film is a semiconductor film, and further comprising:

forming a sacrificial film in said first groove before forming said second film in said first groove; and

removing said sacrificial film after removing said second film to form said second groove.

20. (New) A method for producing a MIS transistor according to claim 18, further comprising:

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polishing a surface of said second film by using said first film as a stopper.

21. (New) A method for producing a MIS transistor according to claim 18, further comprising:

forming a protective film in said second groove before forming said gate insulator film in said second groove.

22. (New) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

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diffusing an impurity on a surface of said semiconductor substrate to form a grooved impurity diffusion region including an elevated impurity diffusion region from a channel region by using said first film as a mask;

forming an insulator film on said grooved impurity diffusion region;

removing said first film so as to form a groove;

forming a gate insulator in said groove so that a top surface of said gate insulator film is arranged farther from said semiconductor substrate than a top surface of said grooved impurity diffusion region; and

forming a gate electrode on a top surface of said gate insulator film.

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23. (New) A method for producing a MIS transistor according to claim 22, further comprising:

elevating said source/drain region by an epitaxial growth technique before diffusing said impurity on said surface of said semiconductor substrate to form said grooved impurity diffusion region including said elevated impurity diffusion region from said channel region by using said first film as a mask.

24. (New) A method for producing a MIS transistor according to claim 23, further comprising:

diffusing an impurity on said surface of said semiconductor substrate before elevating said source/drain region by the epitaxial growth technique.

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25. (New) A method for producing a MIS transistor according to claim 22, wherein said first film is semiconductor film and further comprising:

forming a sacrificial film on a surface of said first film; and

removing said sacrificial film.

26. (New) A method for producing a MIS transistor according to claim 22, further comprising:

forming a protective film in said groove before forming said gate insulator film in said groove.

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27. (New) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

diffusing an impurity on a surface of said semiconductor substrate to form a grooved impurity diffusion region including an elevated impurity diffusion region from a channel region by using said first film as a mask;

forming an insulator film on said grooved impurity diffusion region;

removing said first film so as to form a groove;

forming a gate insulator in said groove and on said insulator film;

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polishing said gate insulator film by using said insulator film as a stopper so that a top surface of said gate insulator film is arranged farther from said semiconductor substrate than a top surface of said grooved impurity diffusion region; and

forming a gate electrode on a top surface of said gate insulator film.

28. (New) A method for producing a MIS transistor according to claim 27, further comprising:

elevating said source/drain region by an epitaxial growth technique before diffusing said impurity on said surface of said semiconductor substrate to form said grooved impurity diffusion region including said elevated impurity diffusion region from said channel region by using said first film as a mask.

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29. (New) A method for producing a MIS transistor according to claim 28, further comprising:

diffusing an impurity on said surface of said semiconductor substrate before elevating said source/drain region by the epitaxial growth technique.

30. (New) A method for producing a MIS transistor according to claim 27, wherein said first film is semiconductor film and further comprising:

forming a sacrificial film on a surface of said first film; and

removing said sacrificial film.

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31. (New) A method for producing a MIS transistor according to claim 27, further comprising:

forming a protective film in said groove before forming said gate insulator film in said groove.

32. (New) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively depositing semiconductor layers serving said source/drain regions so that an inclined surface is formed between the top surface of said semiconductor layers and said channel region;

forming a dummy film on said channel region, which borders said semiconductor layers;

diffusing an impurity on a surface of said semiconductor substrate to form impurity diffusion regions by using said dummy film as a mask and thereafter removing said dummy film;

depositing an insulator film on an exposed surface of said channel region to form a gate insulator film, which has a cross section of a grooved space at a center thereof; and

depositing a gate electrode on a top of said gate insulator film to form a gate electrode having a cross section of a T shape.

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33. (New) A method for producing a MIS transistor according to claim 32, further comprising forming a gate insulator film from said insulator film in said second groove so that a top surface of said gate insulator film is arranged farther from said semiconductor substrate than a top surface of said grooved impurity diffusion region.

34. (New) A MIS transistor comprising: a semiconductor substrate, source/drain regions formed on said semiconductor substrate, a gate insulator, and a gate electrode provided above a channel region,

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wherein top surfaces of said source/drain regions have a substantially flat surface which is elevated from a top surface of said channel region and an inclined surface gradually elevated from said top surface of said channel toward said gate electrode.

35. (New) A MIS transistor according to claim 34, wherein said gate insulator has a larger dielectric constant than that of SiO2.

36. (New) A MIS transistor according to claim 34, wherein said inclined surface is physically separated from said gate electrode by a first insulator.

37. (New) A MIS transistor according to claim 36, wherein said first insulator has a larger dielectric constant than that of SiO2.

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